ABSTRACT

According to one exemplary embodiment, an integrated circuit chip comprises a first interconnect metal layer. The integrated circuit chip further comprises a first intermediate dielectric layer situated over the first interconnect metal layer. The integrated circuit chip further comprises a metal resistor situated over the first intermetallic dielectric layer and below a second intermetallic dielectric layer. The integrated circuit chip further comprises a second interconnect metal layer over the second intermetallic dielectric layer. The integrated circuit chip further comprises a first intermediate via connected to first terminal of the metal resistor, where the first intermediate via is further connected to a first metal segment patterned in the second interconnect metal layer. The integrated circuit chip further comprises a second intermediate via connected to a second terminal of the metal resistor, where the second intermediate via is further connected to a second metal segment patterned in the second interconnect metal layer.